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# FDMA3023PZ

## Dual P-Channel PowerTrench<sup>®</sup> MOSFET

-30 V, -2.9 A, 90 mΩ

### Features

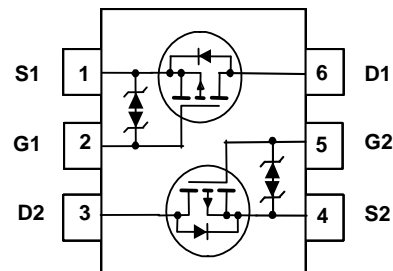
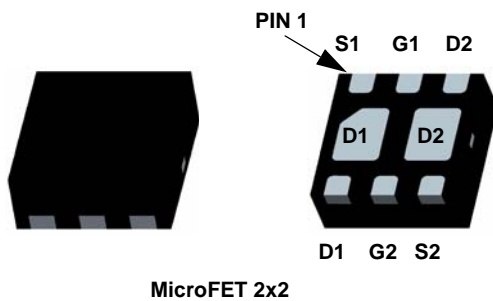
- Max  $r_{DS(on)}$  = 90 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -2.9$  A
- Max  $r_{DS(on)}$  = 130 mΩ at  $V_{GS} = -2.5$  V,  $I_D = -2.6$  A
- Max  $r_{DS(on)}$  = 170 mΩ at  $V_{GS} = -1.8$  V,  $I_D = -1.7$  A
- Max  $r_{DS(on)}$  = 240 mΩ at  $V_{GS} = -1.5$  V,  $I_D = -1.0$  A
- Low profile - 0.8 mm maximum - in the new package MicroFET 2x2 mm
- HBM ESD protection level > 2 kV (Note 3)
- RoHS Compliant
- Free from halogenated compounds and antimony oxides



### General Description

This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra-portable applications. It features two independent P-Channel MOSFETs with low on-state resistance for minimum conduction losses. When connected in the typical common source configuration, bi-directional current flow is possible.

The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-30	V
$V_{GS}$	Gate to Source Voltage	±8	V
$I_D$	Drain Current -Continuous (Note 1a)	-2.9	A
	-Pulsed	-6	
$P_D$	Power Dissipation (Note 1a)	1.4	W
	Power Dissipation (Note 1b)	0.7	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance for Single Operation, Junction to Ambient (Note 1a)	86	°C/W
$R_{\theta JA}$	Thermal Resistance for Single Operation, Junction to Ambient (Note 1b)	173	
$R_{\theta JA}$	Thermal Resistance for Dual Operation, Junction to Ambient (Note 1c)	69	
$R_{\theta JA}$	Thermal Resistance for Dual Operation, Junction to Ambient (Note 1d)	151	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
323	FDMA3023PZ	MicroFET 2X2	7"	8 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-24		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}$ , $V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = -250\text{ }\mu\text{A}$	-0.4	-0.6	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\text{ V}$ , $I_D = -2.9\text{ A}$		71	90	m $\Omega$
		$V_{GS} = -2.5\text{ V}$ , $I_D = -2.6\text{ A}$		97	130	
		$V_{GS} = -1.8\text{ V}$ , $I_D = -1.7\text{ A}$		122	170	
		$V_{GS} = -1.5\text{ V}$ , $I_D = -1.0\text{ A}$		151	240	
		$V_{GS} = -4.5\text{ V}$ , $I_D = -2.9\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		110	140	
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}$ , $I_D = -2.9\text{ A}$		10		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		400	530	pF
$C_{oss}$	Output Capacitance			55	70	pF
$C_{rss}$	Reverse Transfer Capacitance			45	65	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{ V}$ , $I_D = -1.0\text{ A}$ , $V_{GS} = -4.5\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		5	10	ns
$t_r$	Rise Time			4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			62	100	ns
$t_f$	Fall Time			18	33	ns
$Q_{g(TOT)}$	Total Gate Charge			7.9	11	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = -15\text{ V}$ , $I_D = -2.9\text{ A}$		0.9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge	$V_{GS} = -4.5\text{ V}$		1.9		nC

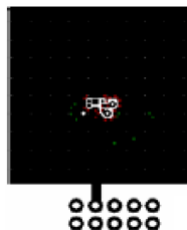
**Drain-Source Diode Characteristics**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-1.1	A
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = -1.1\text{ A}$ (Note 2)		-0.8	-1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -2.9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		18	33	ns
$Q_{rr}$	Reverse Recovery Charge			6.6	13	nC

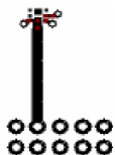
**Notes:**

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.

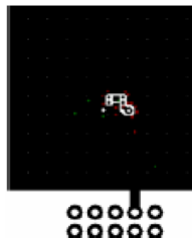
- (a)  $R_{\theta JA} = 86$  °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For single operation.
- (b)  $R_{\theta JA} = 173$  °C/W when mounted on a minimum pad of 2 oz copper. For single operation.
- (c)  $R_{\theta JA} = 69$  °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For dual operation.
- (d)  $R_{\theta JA} = 151$  °C/W when mounted on a minimum pad of 2 oz copper. For dual operation.



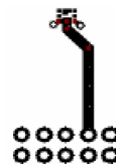
a) 86 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 173 °C/W when mounted on a minimum pad of 2 oz copper.



c) 69 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



d) 151 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

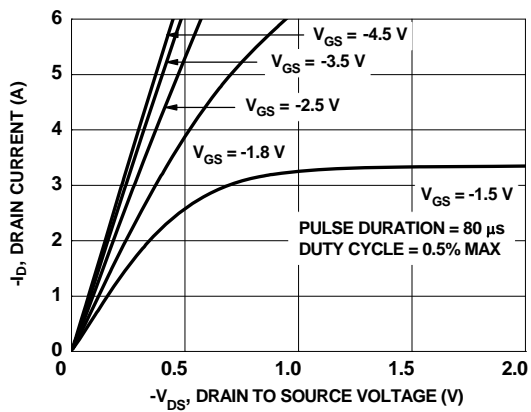


Figure 1. On Region Characteristics

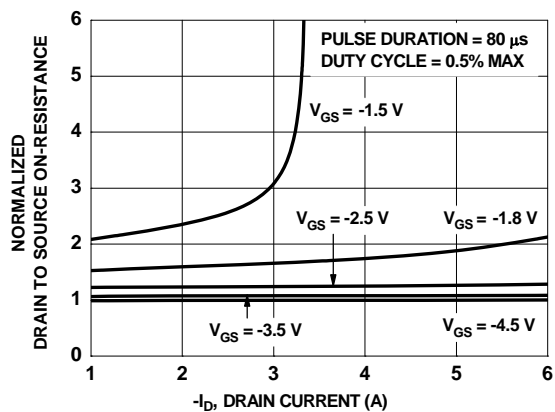


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

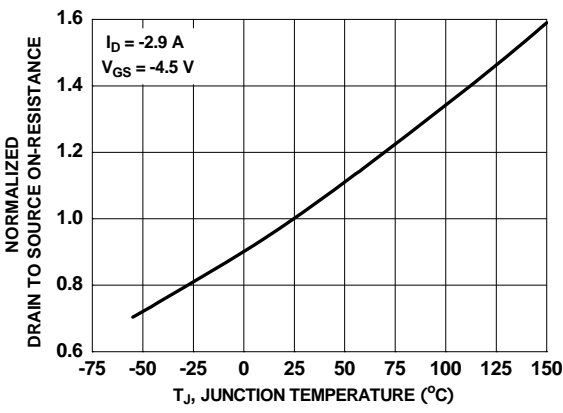


Figure 3. Normalized On Resistance vs Junction Temperature

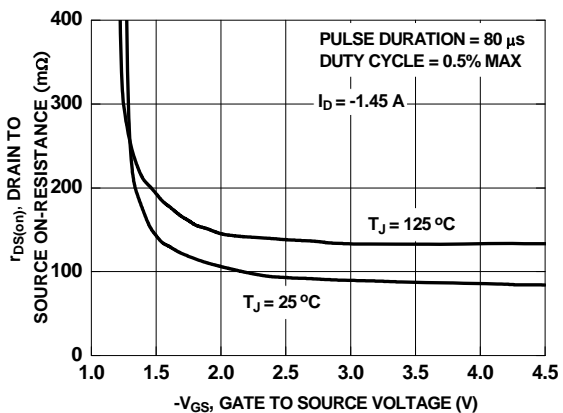


Figure 4. On-Resistance vs Gate to Source Voltage

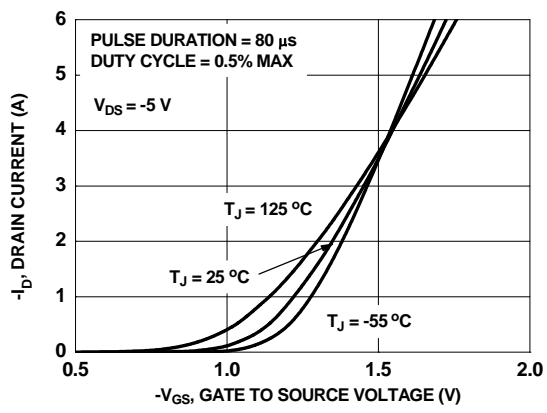


Figure 5. Transfer Characteristics

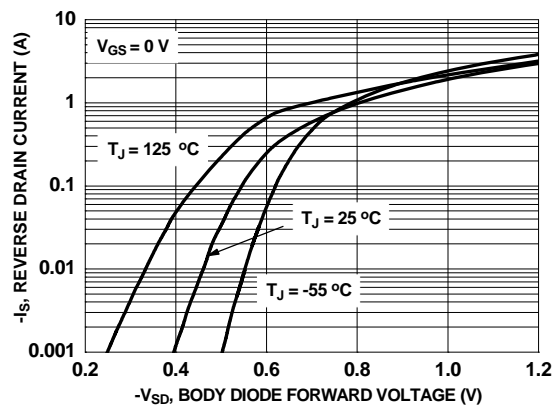
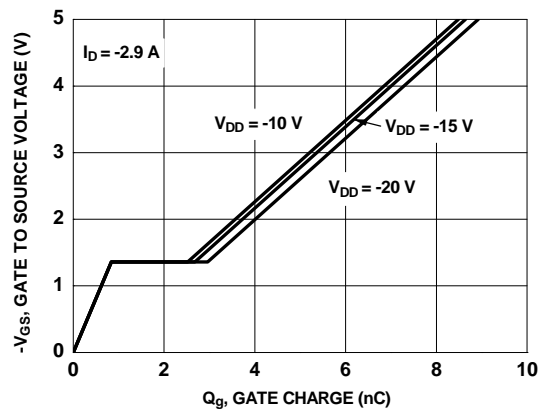
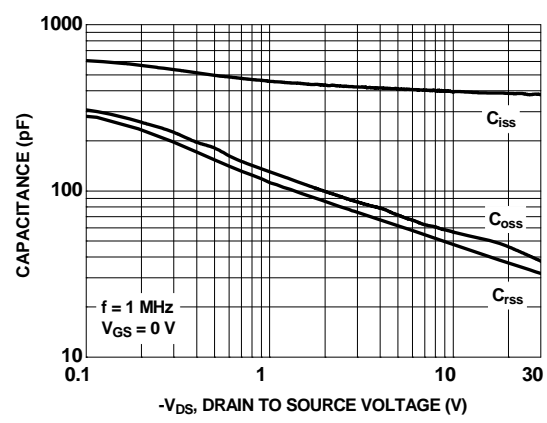


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

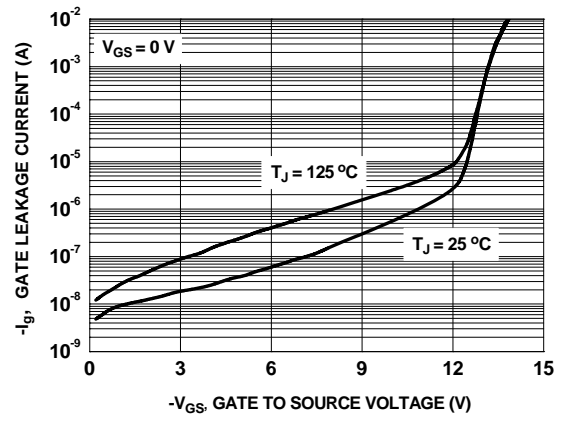
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



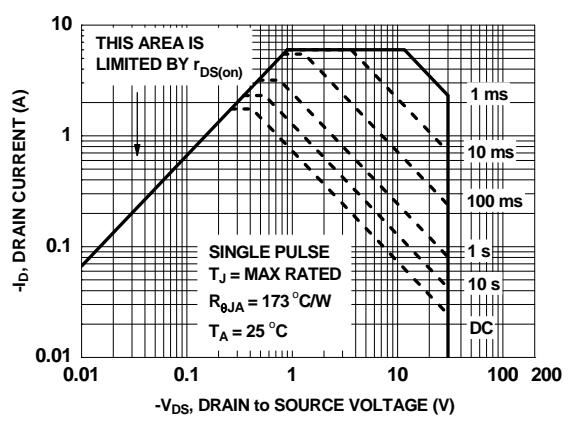
**Figure 7. Gate Charge Characteristics**



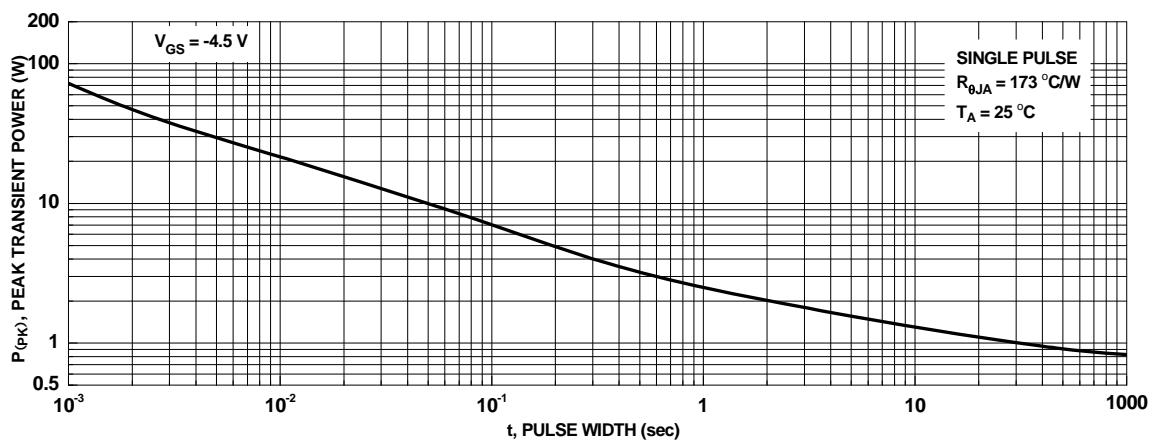
**Figure 8. Capacitance vs Drain to Source Voltage**



**Figure 9. Gate Leakage vs Gate to Source Voltage**

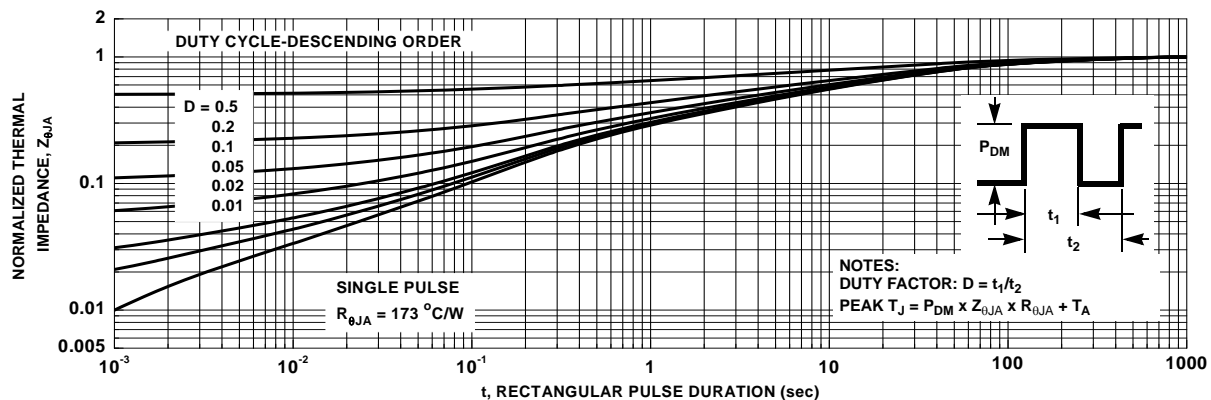


**Figure 10. Forward Bias Safe Operating Area**



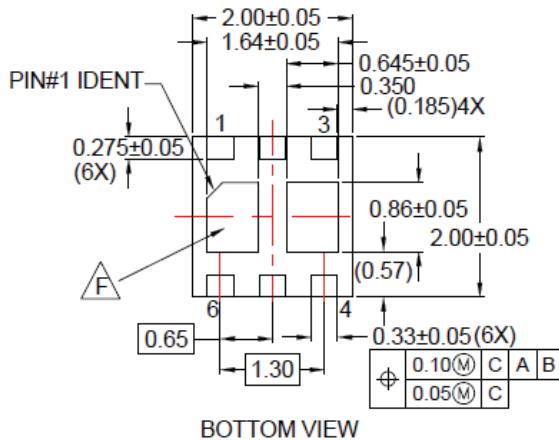
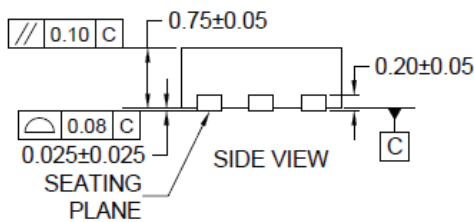
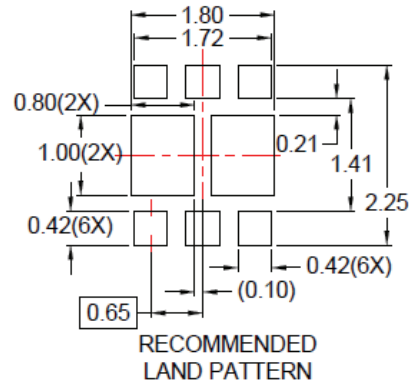
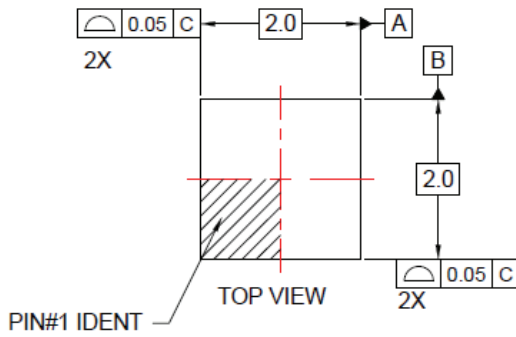
**Figure 11. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout



### NOTES:

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  - DIMENSIONS ARE IN MILLIMETERS.
  - DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
  - LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
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| Build it Now™   | GreenBridge™                                    | Programmable Active Droop™  | TinyCalc™   |
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