PIC16(L)F1614/1618 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1614/1618 family devices that you have received conform functionally to the current Device Data Sheet (DS40001769**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1614/1618 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1614/1618 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>(1,2)	
	DEV<8:0>	Revision ID for Silicon Revision
		A4
PIC16F1614	3078h	4h
PIC16LF1614	307Ah	4h
PIC16F1618	3079h	4h
PIC16LF1618	307Bh	4h

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC12(L)F1612/16(L)F161X Memory Programming Specification"* (DS40001720) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A4
EUSART	Transmit Mode	1.1	Possible duplicate byte transmitted.	X
MSSP	SPI Slave Mode	2.1	SPI Master releasing Slave Select during Slave Sleep mode corrupts data.	X
	SPI Slave Mode	2.2	Receive data lost when Slave Select enable occurs just before Sleep execution.	X
	SPI Slave Mode	2.3	WCOL improperly set during Sleep.	X
ECCP	Compare Mode	3.1	Compare Toggle mode yields unexpected results.	X
FVR	ADC Conversion	4.1	First conversion of FVR signal may contain errors.	X
ADC	Positive Voltage Reference	5.1	Using the FVR as the ADC positive voltage reference can cause missing codes.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Synchronous Asynchronous Receiver Transmitter (EUSART)

1.1 Transmit Mode

Under certain conditions, a byte written to the TXREG register can be transmitted twice. This happens when a byte is written to TXREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register, but also remains in the TXREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around

Method 1: Monitor the Transmit Interrupt Flag bit (TXIF). Writes to the TXREG register can be performed once the TXIF bit is set, indicating that the TXREG register is empty.

Method 2: Monitor the TMRT bit of the TXxSTA register. Writes to the TXREG register can be performed once the TMRT bit is set, indicating that the Transmit Shift Register (TSR) is empty.

Affected Silicon Revisions

A4							
X							

2. Module: Master Synchronous Serial Port (MSSP)

2.1 SPI Slave Mode

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI master releases the $\overline{SS}$ line ($\overline{SS}$ goes high) before the device wakes from Sleep and updates SSPBUF, the received data will be lost.

Work around

Method 1: The SPI master must wait a minimum of parameter SP83 (1.5TCY+40nS) after the last SCK edge AND the addition wake-up time from Sleep before releasing the $\overline{SS}$ line.

Method 2: If both the master and slave devices have an available pin, once the slave has completed the transaction and BF or SSPIF is set, the slave could toggle an output to inform the master that the transaction is complete and that it is safe to release the $\overline{SS}$ line.

Affected Silicon Revisions

A4							
X							

2.2 Receive Data Lost

When the MSSP module is configured in SPI Slave mode with $\overline{SS}$ pin control enabled (SSPM = 0100) and the device is in Sleep mode during SPI activity, if the SPI master enables $\overline{SS}$ ($\overline{SS}$ goes low) within 1 TCY before Sleep is executed, the data written into the SSPBUF by the slave for transmission will remain in the SSPBUF, and the byte received by the slave will be completely discarded. The MSb of the data byte that is currently loaded into SSPBUF will be transmitted on each of the eight SCK clocks, resulting in either a 0x00 or 0xFF to be incorrectly transmitted. This issue typically occurs when the device wakes up from Sleep to process data and immediately goes back to Sleep during the next transmission.

Work around

The SPI slave must wait a minimum of 2.25 TCY from the time the $\overline{SS}$ line becomes active ($\overline{SS}$ goes low) before executing the Sleep command.

Affected Silicon Revisions

A4							
X							

2.3 WCOL Improperly Set During Sleep

When the MSSP module is configured with either of the Slave modes listed below and Sleep is executed during transmission, the WCOL bit is erroneously set. Although the WCOL bit is set, it does not cause a break in transmission or reception.

Mode 1: SPI Slave mode with $\overline{SS}$ disabled (SSPM = 0101) and CKE = 0

Mode 2: SPI Slave mode with $\overline{SS}$ enabled (SSPM = 0100) and $\overline{SS}$ is not set and then cleared before each consecutive transmission. This typically occurs during multiple byte transmissions in which the master does not release the $\overline{SS}$ line until all transmission has completed.

Work around

Method 1: The WCOL bit can be ignored since the issue does not interfere with MSSP hardware.

Method 2: Clear the SSPEN bit after each transaction, the set SSPEN before the next transmission.

Affected Silicon Revisions

A4							
X							

3. Module: Enhanced Capture/Compare/ PWM (ECCP)

3.1 Compare Mode

The ECCP Compare Toggle mode (CCP1M<3:0>bits = 0010) works properly as long as the Timer1 Prescaler value is configured to 1:1. When the Timer1 prescaler value is configured to any other value, the ECCP Compare output yields unexpected results.

Work around

Only use the Compare Toggle mode when the Timer1 prescaler value is set to 1:1.

Affected Silicon Revisions

A4							
X							

4. Module: Fixed Reference Voltage (FVR)

4.1 ADC Conversion

When using the ADC to sample the output of the FVR, the first conversion result may contain errors. This can occur particularly if both the FVR and ADC modules have been powered down for significant time prior to the conversion.

Work around

Method 1: Prior to the conversion, provide “FVR Stabilization Period” per the graph provided in the Electrical Specifications chapter of the data sheet. As shown in this graph, this stabilization time is typically in the range of 25-30 μS. During this stabilization time, the ADC should be enabled and set to sample the VREFL (V_{SS}) node. The following steps should be followed:

1. Enable ADC with sample path set to VREFL (V_{SS});
2. Enable FVR with ADFVR bits set to zero;
3. Configure FVR gain to the desired level per data sheet instructions;
4. Allow time for FVR stabilization. (Poll for FVRRDY = 1);
5. Configure ADC sample path to FVR and required ADC acquisition time allowed;
6. Initiate the ADC conversion.

Method 2: Alternately, the FVR and ADC modules can be enabled and a series of ADC conversion of the sampled FVR output performed while both modules remain active. In this case, the first conversion result should be discarded and the subsequent results utilized. It is noted that this approach, in effect, provides for the stabilization time referred to above.

Affected Silicon Revisions

A4							
X							

5. Module: Analog-to-Digital Converter (ADC)

5.1 Positive Voltage Reference

Using the FVR as the positive voltage reference for the ADC can cause an increase in missing codes.

Work around

Increase the bit conversion time, known as TAD, to 8 μS or higher.

Affected Silicon Revisions

A4							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001769**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (12/2014)

Initial release of this document.

Rev B Document (11/2017)

Added Modules 1 through 5.

Data Sheet Clarifications: Removed Module 1.

Note the following details of the code protection feature on Microchip devices:

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